ABSTRACT OF THE DISCLOSURE

A dual processor system comprises a first processor coupled to a second processor by a system address bus and a data bus. The second processor has a control register having a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory. The control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus. The second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode. This enables both single and burst data transfers between the first processor and the memory of the second processor.